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Attorney Docket No. 20181-5US
Client Ref No. PPA-5

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By: Sunil Dutt

Transmitted herewith for filing is the
[**X**] patent application of

Inventor(s)/Applicant Identifier: Andrew V. Podlesny et al.

For: HIGH SPEED LOW POWER DATA TRANSFER SCHEME

[**X**] This application claims priority from each of the following Application Nos./filing dates:
60/120,531/Filed 2/17/99
the disclosure(s) of which is (are) incorporated by reference.

Enclosed are:
[**X**] 1 sheet(s) of [ ] formal [**X**] informal drawing(s).
[**X**] A [ ] signed [**X**] unsigned Declaration.
[**X**] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [**X**] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

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SF 1068480 v1

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov
Application or Patent No.:
Filed or Issued:
Title: High-Speed Low-Power Data Transfer Scheme

I hereby declare that I am:

[ ] the owner of the small business concern identified below
[X] an official of the small business concern empowered to act on behalf of the concern identified below

Name of Small Business Concern: Elbrus International Limited
Address of Small Business Concern: P.O. Box 265
George Town Grand Cayman, Cayman Islands

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled High-Speed Low-Power Data Transfer Scheme by inventor(s) Andrew V. Podlesny, Alexander V. Malshin and Alexander Y. Solomatnikov described in:

[X] the specification filed herewith;
[ ] Application No. _____, filed _____;
[ ] Patent No. _____, issued _____.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

Name:
Address:

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Alexander K. Kim
Title of Person if Other than Owner: President
Address of Person Signing: 14 Bolshoy Savvinsky per.
Moscow 119435, Russia

Signature _____ Date 02/4/2000

SF 1058186 v1

Attorney Docket No.: 20181-5US
Client Reference No.: PPA-5

PATENT APPLICATION

HIGH SPEED LOW POWER DATA TRANSFER SCHEME

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PATENT
Attorney Docket No.: 20181-5US
Client Reference No.: PPA-5

HIGH SPEED LOW POWER DATA TRANSFER SCHEME

This application claims priority from U.S. Provisional Patent Application No. 60/120,531, filed February 17, 1999, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to a data transfer scheme, and more particularly, to a high speed and low power CMOS data transfer scheme.

2. Description Of The Prior Art

Today's requirements for electronic circuits require high speed. Additionally, the circuits should be as small and simple as possible due to the ever increasing number of circuits that are crowding today's chip devices. Furthermore, circuits for data transfer should not be sensitive to circuit parameter mismatches, noise, and deviations in various applied voltages.

SUMMARY OF THE INVENTION

The present invention provides a high speed and low power CMOS data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver.

In accordance with one embodiment of the present invention, a data transfer arrangement includes two bus drivers, a voltage precharge source, a differential bus coupled to the bus drivers and to the voltage precharge source, and a latching sense amplifier coupled to the differential bus.

In accordance with another embodiment of the present invention, the latching sense amplifier is arranged as a cross coupled latched amplifier.

In accordance with a further embodiment of the present invention, the two bus drivers consist of active pull up/pull down bus drivers.

Thus, the present invention provides a data transfer arrangement that operates at a high speed and uses low power. The data transfer arrangement is faster because the bus voltage swing passes directly to high gain nodes of the cross-coupled latched amplifier. Additionally, the data transfer arrangement uses a lower number of stacked transistors coupled between the supply voltage and the high gain nodes when compared to the prior art. Additionally, the arrangement according to the present invention is less sensitive to deviations in voltage sources and the deviation of threshold voltage concerns of the input transistors. Additionally, the arrangement is less sensitive to circuit parameter mismatches, data bus common mode noise and power bus noises.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred embodiments below, in conjunction with reference to the drawings, in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of a differential data transfer arrangement in accordance with the present invention; and

Figure 2 is a schematic of a circuit for a sense amplifying latch for use in the data transfer arrangement illustrated in Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a data transfer arrangement circuit 10 that includes two bus drivers 11, 12, a precharge circuit 13, and two complementary bus lines 14, 15. The bus lines are inputs to a bus receiver 16 that is arranged as a latching sense amplifier.

The two bus drivers are complementary and consist, preferably, of two active pull up/active pull down bus drivers.

Operation of the data transfer arrangement consists of two phases: A bus precharge phase and a data transfer phase.

During the bus precharge phase, the control input PR (control signal for bus precharge circuit 13) is high and signal inputs DT (true phase of dual-rail data function) and DC (complement phase of dual-rail data function) are low. The true phase driver on transistors 20 and 21 and the complement phase driver on transistors 22 and 23

are in high impedance state and both bus lines are equalized and precharged to a potential V_{pr} (buses precharging voltage level) through the turned on transistors 24, 25 and 26.

During the data transfer phase, the control input PR is low. The signal inputs become differential: DT is high and DC is low, and vise versa. One of the drivers is pulled up and charges the appropriate bus line from the precharged level V_{pr} toward a more positive $V_{dd} - V_t$ (where V_t is the threshold voltage of the pull up NMOS transistor of the driver). At the same time, the other driver is pulled down and discharges the opposite bus line from the precharged level V_{pr} towards a more negative level V_{ss} (ground). This provides a differential voltage: +dV and – dV from the precharging level V_{pr} between true and complement bus lines. To provide proper operation of the bus receiver (the sensing amplifier), the minimum voltage difference 2* dV_{min} (swing) between the lines may be about 0.05-- 0.20V. This low voltage swing is a basis to obtain high frequency of data transfer through the bus.

Figure 2 illustrates sensing amplifier 16. Preferably, the sensing amplifier is a cross-coupled latched amplifier.

The sense amplifier operates in two phases, a precharge phase and a data transfer phase. However, the sensing amplifier operates opposite to analogous phases of the bus driver.

When the control input CLK is low and the bus driver is in the data transfer mode, the sensing amplifier is in the precharge mode. The cross-coupled latched amplifier is isolated from the power buses (transistors 30 and 31 are turned off). Transistors 32 and 33 are turned on and thus, the bus voltage swing passes to the internal nodes IT (positive binary single-rail internal point of the sensing amplifier) and IC (negative binary single-rail data input phase internal point of the sensing amplifier) of the latched amplifier. The output nodes of both dynamic gates are precharged to V_{dd} and the complementary outputs QT (true phase of dual-rail data output signal) and QC (complement phase of dual-rail output data signal) of the sensing amplifier become high.

When the control input CLK is high and the bus driver is in the precharge mode, the sensing amplifier is in the data transfer mode. Transistors 32 and 33 are turned of and isolate the internal nodes IT and IC of the latched amplifier from the bus lines. The cross-coupled latched amplifier is connected to power buses (transistors 30 and 31 are turned on) and it begins to amplify the low voltage swings of the internal nodes IT

and IC to full logic levels. The output node of one of the dynamic gates is discharged to ground and the appropriate output QT or QC of the sensing amplifier becomes low.

The use of domino output stages in accordance with the present invention instead of static inverters is necessary to avoid leakage currents and output glitches, which may appear because potentials of nodes IT and IC are approximately equal to V_{pr} during the operating cycle of the bus driver. Weak PMOS transistors 34 and 35 are preferably included in the sensing amplifier to help prevent output glitches.

The data transfer arrangement in accordance with the present invention provides an increase in speed due to the differential low voltage swing bus driver in combination with the use of the latched differential sense amplifier as the bus receiver.

A further increase in speed is attained with the data transfer arrangement due to the pull up/pull down bus drivers, which provide equal low differential voltage swings +dV/ - dV in both bus lines. This allows both bus lines to be active during the data transfer phase, eliminates the necessity to use special circuits for holding the precharged level and leads to a reduction in the capacitance load of the driver.

The buses precharging to the specific level between ground and V_d ($V_{pr} = K*V_{dd}$, where K = 1/3 for the ideal MOS model) also provides: equal charge and discharge driver currents $I_{ch} = Id_{ch}$, provided by the NMOS pull up follower and the NMOS pull down switch, respectively, and therefore, equal differential voltage swings dV in both charged and discharged bus during the data transfer phase Pdtf: + dV = $I_{ch}*D_{dtf}/C_{LOAD}$; and -dV = $I_{dch}*T_{dtf}/C_{LOAD}$. I_{ch} represents the driver pull up output current (which provides the C_{LOAD} charging from V_{pr} up to V_{dd}); I_{dch} represents the driver pull down output current (providing the C_{LOAD} discharging from V_{pr} up to V_{ss}); C_{LOAD} represents the bus lines' compacitances; +dV represents the bus voltage change up from V_{pr} during data transfer phase; -dV represents the bus voltage change down from V_{pr} during data transfer phase; and T_{dtf} represents the data transfer phase duration. The buses precharging to the specific level between ground and V_{dd} also provides high noise immunity due to active mode for both buses that equal low output resistances of the drivers in pull up and pull down mode and; low total power consumed by drivers during the cycle of operation (transfer plus precharge).

The latched sense amplifier is faster due to the bus voltage swing passing directly to the high-gain nodes IT and IC of the cross- coupled latched amplifier, the lower number of stacked transistors that are connected between the supply voltage V_{dd} (or

V_{cc}) and nodes IT and IC, the fact that during latching of the IT and IC nodes, the nodes are charged by $K*V_{dd}$ and $(1-K)*V_{dd}$ instead of simply V_{dd}. Additionally, the speed of the latched sensing amplifier is effected little by the deviation of voltage V_{pr} and the deviation of the threshold voltage of the input transistors.

In addition to the higher speed and low power consumption of the data transfer arrangement in accordance with the present invention, the arrangement is also less sensitive to circuit parameters mismatching, data bus common mode noise and power buses' noises since both drivers are active during data transfer phase. During the appropriate bus precharge phase, the bus receiver is isolated from the bus lines.

Although the invention has been described with reference to specific exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

a latching sense amplifier coupled to the differential bus.

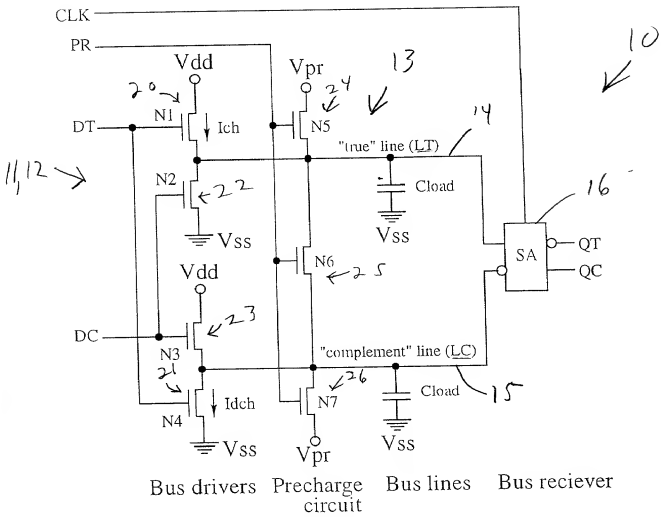
2. A data transfer arrangement in accordance with claim 1 wherein the latching sense amplifier comprises a cross coupled latched amplifier.

3. A data transfer arrangement in accordance with claim 1 wherein the bus drivers consist of active pull up/pull down bus drivers.

HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME

ABSTRACT OF THE DISCLOSURE

A data transfer arrangement. The data transfer arrangement includes two active pull up/active pull down bus drivers and a voltage precharge source. A differential bus is coupled to the bus drivers and to the voltage precharge source. A latching sense amplifier is coupled to the differential bus and serves as the bus receiver. The bus drivers operate in a precharge phase and a data transfer phase. The bus receiver operates in an analogous but opposite manner, i.e., when the bus drivers are in the precharge phase, the bus receiver is in the data transfer phase and when the bus drivers are in the data transfer phase, the bus receiver is in a precharge phase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QC
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Vpr
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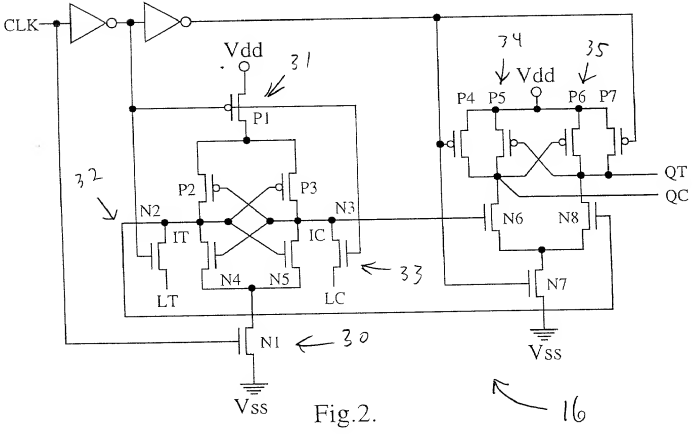
Bus drivers
Precharge circuit
Bus lines
Bus reciever

Fig.1.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N2
N3
N6
N8
IT
IC
33
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N5
N7
LT
LC
N1
30
Vss
Vss
16

Fig.2.

DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: HIGH-SPEED LOW-POWER DATA TRANSFER SCHEME, the specification of which __X__ is attached hereto or ____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/120,531	February 17, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Date	Date	Date

SF 1060790 v1